



1 IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2 EXAMINER: NGUYEN, THINH T.

3 APPLICANTS: JAMIN LING, ET AL.

4 SERIAL NO.: 09/766,798

5 FILED: Jan. 22, 2001

6 FOR: "ELECTROLESS Ni/Pd/Au METALLIZATION  
7 STRUCTURE FOR COPPER INTERCONNECT  
SUBSTRATE AND METHOD THEREFOR"

Art Unit 2818

6/a  
J. Marley  
4-8-02

8 I hereby certify that this correspondence is being deposited with the United  
9 States Postal Service as first class mail in an envelope addressed to:  
Commissioner for Patents, Washington, D.C. 20231 on: March 21, 2002  
10 Marvin A. Glazer

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Signature

12 March 21, 2002

Date

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13 **AMENDMENT**

14 Honorable Commissioner for Patents  
15 Washington, D.C. 20231

16 Sir:

17 In response to the Office Action mailed on December 5, 2001, please amend the above-  
18 identified patent application as follows:

19 **In the Claims:**

20 Amend claim 1 as follows:

21 1. (Amended) An integrated circuit structure comprising in combination:

- 22 a. a semiconductor wafer having an upper surface, the semiconductor wafer having a  
23 plurality of identical die formed therein, each of the identical die having a plurality of  
24 semiconductor devices formed therein upon the surface of the semiconductor wafer;  
25 b. a patterned layer of interconnect metal formed upon the upper surface of the  
26 semiconductor wafer for electrically interconnecting the plurality of semiconductor devices  
27 formed within each such die, said patterned layer of interconnect metal including connection  
28 pads for making electrical connection to circuitry external to the semiconductor wafer;

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